I CLAIM:

1. A method of programming a floating-gate field-effect transistor ("FET") in which first and second source/drain regions are separated from each other by a channel portion of a body region that forms a pn junction with each source/drain region, a floating-gate electrode laterally adjacent to the first source/drain region overlies a first part of the channel portion, and a select-gate electrode laterally adjacent to the second source/drain region and spaced apart from the floating-gate electrode overlies a second part of the channel portion lateral to the first part of the channel portion, the FET initially being in an erased condition with a programmable threshold voltage (a) less than a first transition value V_{T1} if the FET is of n-channel type and (b) greater than $-V_{T1}$ if the FET is of p-channel type, the FET being selectively placable in a programmed condition with the programmable threshold voltage (a) greater than a second transition value V_{T2} if the FET is of n-channel type and (b) less than $-V_{T2}$ if the FET is of p-channel type where V_{T2} exceeds or equals V_{T1}, the method comprising:

changing a first voltage applied to the first source/drain region from a nominal first value to a programming first value;

controlling a second voltage applied to the second source/drain region so as to (a) change from a nominal second value to a programming-inhibit second value if the FET is to remain in its erased condition and (b) stay largely at the nominal second value if the FET is to be placed in its programmed condition; and

changing a select voltage applied to the select-gate electrode from a nominal select value to a programming-enable select value such that, in an instance where the FET is to remain in its erased condition, the select voltage starts to change from its nominal value to the programming-enable value after the second voltage starts to change from its nominal value to the programming-inhibit value and such that the FET (a) remains in the erased condition if the second voltage goes to its programming-inhibit value or (b) enters the programmed condition if the second voltage stays largely at its nominal value.

2. A method as in Claim 1 wherein the select voltage starts to change from its nominal value to the programming-enable value after the first voltage starts to change from its nominal value to its programming value.

3. A method as in Claim 1 further including subsequent to the changing and controlling acts:

changing the select voltage from its programming-enable value back largely to its nominal value;

changing the first voltage from its programming value back largely to its nominal value; and

controlling the second voltage so as to (a) change from its programming-inhibit value back largely to its nominal value if the second voltage earlier changed from its nominal value to its programming-inhibit value and (b) otherwise stay largely at its nominal value such that, in an instance where the second voltage changes from its programming-inhibit value back largely to its nominal value, the select voltage starts to change from its programming-enable value back largely to its nominal value before the second voltage starts to change from its programming-inhibit value back largely to its nominal value.

4. A method as in Claim 3 wherein the select voltage starts to change from its programming-enable value back largely to its nominal value before the first voltage starts to change from its programming value back largely to its nominal value.

5. A method as in Claim 1 wherein:

the FET is a memory element that operates between a low supply voltage and a high supply voltage during reading of the memory element;

the programming value is (a) greater than the high supply voltage if the FET is of n-channel type and (b) less than the high supply voltage if the FET is of p-channel type;

the programming-inhibit and programming-enable values are both (a) greater than the low supply voltage if the FET is of n-channel type and (b) less than the high supply voltage if the FET is of p-channel type; and

the programming-inhibit value is (a) greater than the programming-enable value if the FET is of n-channel type and (b) less than the programming-enable value if the FET is of p-channel type.

6. A method as in Claim 5 wherein the nominal values are all largely equal to one another.

7. A method as in Claim 1 wherein a control-gate electrode overlies the floating-gate electrode above the first part of the channel portion and is spaced apart from the select-gate electrode, the method further including changing a control voltage applied to the control-gate electrode from a nominal control value to a programming control value.

8. A method as in Claim 7 wherein the select voltage starts to change from its nominal value to its programming-enable value after the first and control voltages start to change from their nominal values to their programming values.

9. A method as in Claim 7 wherein the select voltage starts to change from its nominal value to its programming-enable value after at least one of the first and control voltages has changed at least 50% from its nominal value to its programming value.

10. A method as in Claim 7 wherein, in an instance where the FET is to remain in the erased condition, the select voltage starts to change from its nominal value to its programming-enable value after the second voltage largely reaches the programming-inhibit value.

11. A method as in Claim 7 further including subsequent to the changing and controlling acts:

changing the select voltage from its programming-enable value back largely to its nominal value;

changing the first and control voltages from their programming values back largely to their nominal values; and

controlling the second voltage so as to (a) change from its programming-inhibit value back largely to its nominal value if the second voltage earlier changed from its nominal value to its programming-inhibit value and (b) otherwise stay largely at its nominal value such that, in an instance where the second voltage changes from its programming-inhibit value back largely to its nominal value, the select voltage starts to change from its programming-enable value back largely to its nominal value before the second voltage starts to change from its programming-inhibit value back largely to its nominal value.

12. A method as in Claim 11 wherein the select voltage starts to change from its programming-enable value back largely to its nominal value before the first and control voltages start to change from their programming values back largely to their nominal values.

13. A method as in Claim 11 where, in an instance where the second voltage changes from its programming-inhibit value back largely to its nominal value, the select voltage substantially completes changing from its programming-enable value back largely to its nominal value before the second voltage starts to change from its programming-inhibit value back largely to its nominal value.

14. A method as in Claim 7 wherein:

the FET is a memory element that operates between a low supply voltage and a high supply voltage during reading of the memory element;

each programming value is (a) greater than the high supply voltage if the FET is of n-channel type and (b) less than the high supply voltage if the FET is of p-channel type;

the programming-inhibit and programming-enable values are both (a) greater than the low supply voltage if the FET is of n-channel type and (b) less than the high supply voltage if the FET is of p-channel type; and

the programming-inhibit value is (a) greater than the programming-enable value if the FET is of n-channel type and (b) less than the programming-enable value if the FET is of p-channel type.

15. A method as in Claim 14 wherein the nominal values are all largely equal to (a) the low supply voltage if the FET is of n-channel type and (b) the high supply voltage if the FET is of p-channel type.

16. A method as in Claim 7 wherein, for a specified voltage difference between the first and control voltages, an inversion layer (a) occurs in the first part of the channel portion when the FET is in the erased condition and (b) does not occur there when the FET is in the programmed condition.

17. A method as in Claim 1 wherein the select-gate electrode extends over the floating-gate electrode above the first part of the channel portion.

18. A method as in Claim 1 wherein V_{T2} exceeds V_{T1}.

19. A method as in Claim 1 wherein the FET is of n-channel type.

20. A method as in Claim 19 wherein:

the changing acts comprise raising the first and control voltages from their nominal values respectively to their programming and programming-enable values; and

the controlling act comprises raising the second voltage from its nominal value to the programming-inhibit value if the FET is to remain in the erased condition.

21. A method of programming a group of memory elements respectively comprising like-polarity floating-gate field-effect transistors ("FETs") of an erasable programmable read-only memory in which each FET has (a) first and second source/drain regions laterally separated from each other by a channel portion of a body region that forms a pn junction with each source/drain region, (b) a floating-gate electrode laterally adjacent to the first source/drain region and overlying a first part of the channel portion, and (c) a select-gate electrode laterally adjacent to the second source/drain region, spaced apart from the floating-gate electrode, and overlying a

second part of the channel portion lateral to the first portion of the channel portion, each FET being in an erased condition when its programmable threshold voltage is (a) less than a first transition value V_{T1} if that FET is of n-channel type and (b) greater than $-V_{T1}$ if that FET is of p-channel type, each FET being in a programmed condition when its programmable threshold voltage is (a) greater than a second transition value V_{T2} if that FET is of n-channel type and (b) less than $-V_{T2}$ if that FET is of p-channel type where V_{T2} exceeds or equals V_{T1}, the method comprising:

selecting a group of the FETs that are initially in their erased conditions and are to be selectively placed in their programmed conditions;

changing first voltages applied respectively to the first source/drain regions of the selected FETs from respective nominal first values to respective programming first values;

controlling second voltages applied respectively to the second source/drain regions of the selected FETs so that the second voltage for each selected FET (a) changes from a nominal second value to a programming-inhibit value if that FET is to remain in its erased condition and (b) stays largely at the nominal second value if that FET is to be placed in the programmed condition; and

changing select voltages respectively applied to the select-gate electrodes of the selected FETs from respective nominal select values to respective programming-enable select values such that, in each instance where one of the selected FETs is to remain in its erased condition, the select voltage for that selected FET starts to change from the nominal value for that select voltage to its programming-enable value after the second voltage for that selected FET starts to change from the nominal value for that second voltage to its programming-inhibit value and such that each selected FET (a) remains in its erased condition if its second voltage goes to that second voltage's programming-inhibit value and (b) enters its programming condition if its second voltage stays largely at that second voltage's nominal value.

22. A method as in Claim 21 wherein the select voltages all start to change from their nominal values to their programming-enable values after the first voltages all start to change from their nominal values to their programming values.

23. A method as in Claim 22 wherein each FET includes a control-gate electrode which overlies its floating-gate electrode above the first part of its channel portion and is spaced apart from its select-gate electrode, the method further including changing control voltages applied respectively to the control-gate electrodes from respective nominal control values to respective programming control values.

24. A method as in Claim 23 wherein the select voltages all start to change from their nominal values to their programming-enable values after the first and control voltages all start to change from their nominal values to their programming values.

25. An electronic circuit comprising:

a floating-gate field-effect transistor ("FET") which comprises (a) first and second source/drain regions laterally separated from each other by a channel portion of a body region that forms a pn junction with each source/drain region, (b) a floating-gate electrode laterally adjacent to the first source/drain region and overlying a first part of the channel portion, and (c) a select-gate electrode laterally adjacent to the second source/drain region, spaced apart from the floating-gate electrode, and overlying a second part of the channel portion lateral to the first part of the channel portion, the FET being in an erased condition when its programmable threshold voltage is (a) less than a first transition value V_{T1} if the FET is of n-channel type and (b) greater than $-V_{T1}$ if the FET is of p-channel type, the FET being in a programmed condition when its programmable threshold voltage is (a) greater than a second transition value V_{T2} if the FET is of n-channel type and (b) less than $-V_{T2}$ if the FET is of p-channel type where V_{T2} exceeds or equals V_{T1};

first control circuitry which applies a first voltage to the first source/drain region and is operable to change the first voltage from a nominal first value to a programming first value during a programming operation;

second control circuitry which applies a second voltage to the second source/drain region and is operable (a) to change the second voltage from a nominal second value to a programming-inhibit second value during a programming operation if the FET is initially in the erased condition and is to remain in the erased condition and (b) to maintain the second voltage largely at the nominal second value during the programming operation if the FET is to be placed in its programmed condition; and

select-gate control circuitry which applies a select voltage to the select-gate electrode and is operable to change the select voltage from a nominal select value to a programming-enable select value during a programming operation such that, during a programming operation in an instance where the FET is to remain in the erased condition, the select voltage starts to change from its nominal value to its programming-enable value after the second voltage starts to change from its nominal value to its programming-inhibit value and such that, when the FET was in the erased condition prior to the programming operation, the FET (a) remains in the erased condition during that programming operation if the second voltage goes to its programming-inhibit value during that programming operation and (b) enters the programmed condition during that

programming operation if the second voltage stays largely at its nominal value during that programming operation.

26. A circuit as in Claim 25 wherein, during a programming operation, the select voltage starts to change from its nominal value to the programming-enable value after the first voltage starts to change from its nominal value to its programming value.

27. A circuit as in Claim 25 wherein the FET includes a control-gate electrode overlying the floating-gate electrode above the first part of the channel portion and spaced apart from the select-gate electrode, the circuit further including control-gate control circuitry which applies a control voltage to the control-gate electrode and is operable to change the control voltage from a nominal control value to a programming control value during a programming operation.

28. A circuit as in Claim 27 wherein, during a programming operation, the select voltage starts to change from its nominal value to the programming-enable value after the first voltage starts to change from its nominal value to its programming value.

29. A circuit as in Claim 27 wherein, for a specified voltage difference between the first and control voltages, an inversion layer (a) occurs in the first part of the channel portion when the FET is in the erased condition and (b) does not occur there when the FET is in the programmed condition.

30. A circuit as in Claim 25 the select-gate electrode extends over the floating-gate above the first part of the channel portion.

31. An erasable programmable read-only memory ("EPROM") comprising:

a group of memory elements respectively comprising like-polarity floating-gate field-effect transistors ("FETs") wherein each FET comprises (a) first and second source/drain regions laterally separated from each other by a channel portion of a body region that forms a pn junction with each source/drain region, (b) a floating-gate electrode laterally adjacent to the first source/drain region and overlying a first part of the channel portion, and (c) a select-gate electrode laterally adjacent to the second source/drain region, spaced apart from the floating-gate electrode, and overlying a second part of the channel portion lateral to the first part of the channel portion, each FET being in an erased condition when its programmable threshold voltage is (a) less than a first transition value V_{T1} if that FET is of n-channel type and (b) greater than $-V_{T1}$ if that FET is of p-channel type, each FET being in a programmed condition when its

programmable threshold voltage is (a) greater than a second transition value V_{T2} if that FET is of n-channel type and (b) less than $-V_{T2}$ if that FET is of p-channel type where V_{T2} exceeds or equals V_{T1};

first control circuitry which applies first voltages respectively to the first source/drain regions and is operable to change the first voltage for each FET from a nominal first value to a programming first value during a programming operation for that FET;

second control circuitry which applies second voltages respectively to the second source/drain regions and is operable (a) to change the second voltage for each FET from a nominal second value to a programming second value during a programming operation for that FET if it is initially in its erased condition and is to remain in its erased condition during that programming operation and (b) to maintain the second voltage for each FET largely at the nominal value for that second voltage during the programming operation if that FET is to be placed in its programmed condition during that programming operation; and

select-gate control circuitry which applies select voltages respectively to the select-gate electrodes and is operable to change the select voltage for each FET from a nominal select value to a programming select value during a programming operation for that FET such that, during a programming operation for a selected group of the FETs in an instance where one of the selected FETs is initially in its erased condition and is to remain in its erased condition, the select voltage for the selected FET starts changing from the nominal value for that select voltage to its programming-enable value after the second voltage for that selected FET starts changing from the nominal value for that second voltage to its programming-inhibit value and such that, when each selected FET was in its erased condition prior to the programming operation for that selected FET, it (a) remains in its erased condition during that programming operation if its second voltage goes to the programming-inhibit value for that second voltage during that programming operation and (b) enters its programmed condition during that programming operation if its second voltage stays largely at the nominal value for that second voltage during that programming operation.

32. An EPROM as in Claim 31 wherein, during a programming operation, the select voltages all start to change from their nominal values to their programming-enable values after the first voltages all start to change from their nominal values to their programming values.

33. An EPROM as in Claim 31 wherein a control-gate electrode of each FET overlies its floating-gate electrode above the first part of its channel portion and is spaced apart from its select-gate electrode, the EPROM further including control-gate circuitry which applies control

voltages respectively to the control-gate electrodes and is operable to change the control voltage for each FET from a nominal control value to a programming control voltage during a programming operation for that FET.

34. An EPROM as in Claim 33 wherein, during a programming operation, the select voltages all start to change from their nominal values to their programming-enable values after the first and control voltages all start to change from their nominal values to their programming values.